ABSTRACT OF THE DISCLOSURE

A virtual channel buffer of a transaction scheduler in a computer system I/O node. A control unit includes a plurality of scheduler units. Each scheduler unit may include a first and a second buffer circuit. The first buffer circuit may include a first plurality of buffers and the second buffer circuit may include a second plurality of buffers, each of which are coupled to receive control commands from a first and second source, respectively. Each buffer of the first and the second plurality of buffers corresponds to a respective virtual channel of a plurality of virtual channels and may be configured for storing selected control commands that belong to said respective virtual channels. Each scheduler unit may also include an arbitration unit for arbitrating between the control commands stored in the first buffer circuit and the control commands stored in the second buffer circuit.